REMARKS

Claims 1-13 are pending. Claims 1 and 10 have been amended to delete the redundant word "any" in line 5. It is submitted that the claim amendment does not narrow the scope of the claims for reasons related to the statutory requirements for a patent.

Claims 1-5 and 10-12 have been rejected under 35 U.S.C. §102(a) as being anticipated by the Applicants' Admitted Prior Art (AARA). Claims 6-9 and 13 have been rejected under 35 U.S.C. §103(a) as being unpatentable over the AABA, These rejections are respectfully traversed.

Claim 1 recites a bi-directional bus circuitry shared among a plurality of circuit blocks, comprising:

a data bus divided into (J + 1) (J: natural number being 1 or more than 1) bus nodes,

each of said plurality of circuit blocks being connected to one of said (J + 1) bus nodes;

a potential fixing circuit provided corresponding to one of said (J + 1) bus nodes, for setting potential level of corresponding said bus node to a prescribed potential when data is input to/output from none of said plurality of circuit blocks;

J repeater circuits provided between adjacent said bus nodes respectively,

each repeater circuit having

a first signal transmitting circuit transmitting data from one to the other of said adjacent bus nodes, and

a second signal transmitting circuit transmitting data from said the other to said one of said adjacent bus nodes; and

an arbiter circuit receiving circuit block information for specifying a circuit block which is an object of data output, and controlling activation of said first and second signal transmitting circuits. The arbiter circuit activates, when said data is input to/output from none of said plurality of circuit blocks, either one of said first and second signal transmitting circuits in each repeater circuit, so that potential level of said bus node corresponding to said potential fixing circuit is transmitted to said data bus entirely.

Independent claim 10 recites that the arbiter circuit activates both of the first and second signal transmitting circuits in each of the repeater circuits when the data bus is not used, that is, when data is input to/output from none of the plurality of circuit blocks.

As demonstrated below, the AAPA does not disclose or suggest the potential fixing circuit provided corresponding to one of the (J + 1) bus nodes, for setting potential level of corresponding bus node to a prescribed potential when data is input to/output from none of the plurality of circuit blocks, as claim 1 recites.

Further, the AAPA does not disclose or suggest the arbiter circuit that activates, when the data is input to/output from none of the plurality of circuit blocks, either one of the first and second signal transmitting circuits in each repeater circuit, so that potential level of said bus node corresponding to the potential fixing circuit is transmitted to said data bus entirely, as claim 1 requires.

Moreover, the AAPA does not disclose or suggest the repeater circuit including a first signal transmitting circuit, a second signal transmitting circuit and an arbiter circuit that activates both of the first and second signal transmitting circuits in each of the repeater circuits when the data bus is not used, as recited in independent claim 10.

REJECTIONS OF CLAIMS 1-9

The AAPA discusses a block diagram of a conventional bi-directional bus circuit (see Fig. 9), and a schematic diagram of a conventional mono-directional bus circuit (see Fig. 10).

As shown in Fig. 9 and disclosed on pages 1-3 of the present application, the conventional bi-directional bus circuitry **500** includes a first pair of circuit blocks **10-a** and **10-b** coupled to a second pair of circuit blocks **10-c** to **10-d** via a repeater circuit **50** and bus nodes **Nb1** and Nb2. The circuit blocks **10-a** to **10-d** each include respective input buffers **12-a** to **12-d** and respective output buffers **14-a** to **14-d**, and the repeater circuit **50** includes tristate buffers **51** and **52** that amplify and transmit a signals between bus nodes **Nb1** and **Nb2**. See page 2 lines 1-9.

The various buffers **12-a** to **12-d**, **14-a** to **14-d**, and **51-52** are either in an active (on) state, i.e., transmitting either a logic high or logic low level, or in a high-impedance (off) state, depending on the states of signals **CSBa** to **CSBd** emanating from arbiter circuit **520**. See page 2, lines 9-19. However, Fig. 9 does not disclose any bi-directional bus circuitry with a potential fixing circuit for setting the potential level of various bus node to a prescribed potential when data is not input to or output from any of a plurality of circuit blocks, as recited in independent claim 1.

To the contrary, as specifically recited on page 3, lines 7-15, the bus nodes **Nb1** and **Nb2** are not fixed when the data bus is unused, but are in a floating state. As a result, the potential of bus nodes **Nb1** and **Nb2** can either settle to an intermediate level, which can result in an unnecessary current drain, or possibly reach voltages beyond power and ground levels, which can cause damage to the circuitry **500**. See page 3, lines 16-25.

In comparison with the bi-directional circuitry of Fig. 9, the present invention can fix an otherwise floating node to a fixed level, such as a ground or power level (see Figs. 1 and 4), thus preventing the power drain or circuitry damage problems of the bi-directional circuitry **500** of Fig. 9. Thus, Fig. 9 does not teach or suggest any bi-directional bus circuitry with a potential fixing circuit for setting the potential level of unused bus nodes, as required by independent claim 1.

Figure 10 discloses a schematic diagram of conventional **mono-directional** bus circuitry **600** that includes NOR GATE **GC1** and transistor **QTN**, which enable circuitry **600** to fix the outputs of buffers **GI1-GIn** when circuitry **600** is unused. See page 3, line 30 to page 4, line 12. However, as explicitly disclosed in the specification, the **mono-directional** bus circuitry **600** of Fig. 10 is a distinctly different circuit than the **bi-directional** bus circuitry **500** of Fig. 9. As Fig. 10 relates only to mono-directional bus circuitry, Fig. 10 consequently does not teach or suggest any bi-directional bus circuitry with a potential fixing circuit for setting the potential level of unused bus nodes, as required by independent claim 1.

Further, the background art in Figs. 9 and 10 neither discloses nor suggests the arbiter circuit recited in claim 1. When the data is input to/output from none of the plurality of circuit blocks, the claimed arbiter circuit activates either one of the first and second signal transmitting circuits in each repeater circuit, so that potential level of the bus node corresponding to the potential fixing circuit is transmitted to the data bus entirely.

As described in the specification, page 14, lines 7 to 21, the provision of such an arbiter circuit can reduce the number of potential fixing circuits, and can reduce data bus parasitic capacitance. As a result, the data rate may be increased.

By contrast, the background art does not teach or suggest the arbiter circuit that interacts with the potential fixing circuit to activate one of the first and second signal transmitting circuits in each repeater circuit, so that potential level of the bus node corresponding to the potential fixing circuit is transmitted to the data bus entirely, as claim 1 requires.

Furthermore, not only is **mono-directional** bus circuitry **600** different circuit than the **bi-directional** bus circuitry **500**, but the AAPA provides no direction or motivation to modify the bi-directional bus circuitry **500** of Fig. 9 to incorporate ANY technique for fixing potential for buses in use. In fact, the AAPA teaches away from such a modification due to inherent difficulties. See, page 4, lines 12-17. Therefore, not only does the AAPA fail to anticipate the invention recited in claim 1 35 U.S.C. §102, but there can be no foundation for a *prima facie* case of obviousness under 35 U.S.C. §103.

Thus, independent claim 1 is directed to patentable subject matter. Dependent claims 2-9 are directed to patentable subject matter by virtue of their dependency as well as for the additional features they recite. Accordingly, withdrawal of the rejections of claims 1-9 is respectfully requested.

REJECTIONS OF CLAIMS 10-13

Applicants assert that the AAPA does not teach, suggest or otherwise make obvious a **bi-directional** bus circuitry shared among a plurality of circuit blocks that includes a data bus divided into a plurality of bus nodes, repeater circuits arranged between adjacent bus nodes with each repeater including a first signal transmitting circuit, a second signal transmitting circuit and an arbiter circuit that activates both of the first and second signal

transmitting circuits in each of the repeater circuits **when the data bus is not used**, as recited in independent claim 10.

As discussed above, Fig. 9 does not disclose any form of arbiter circuit that activates both a first and (opposing) second signal transmitting circuits in a repeater circuit **when the data bus is not used**. To the contrary, as specifically recited in the AAPA, when the data bus of Fig. 9 is unused, BOTH "tri-state buffers **51** and **52** in repeater circuit **50** are all set to the high impedance state, so that bus nodes **Nb1** and **Nb2** both come to have potential levels not fixed." See, page 3, lines 7-15. Thus, Fig. 9 does not teach or suggest each and every feature recited in independent claim 10.

As discussed above, Fig. 10 does not disclose any form of bi-directional bus circuitry, much less any form of arbitration circuitry useable to control a first and (opposing) second signal transmitting circuits in a repeater circuit when the data bus is not used. Thus, the circuitry **600** of Fig. 10 does not provide for the deficiencies of Fig. 9

Thus, independent claim 10 is directed to patentable subject matter. Dependent claims 12-13 are directed to patentable subject matter by virtue of their dependency as well as for the additional features they recite. Accordingly, withdrawal of the rejections of claims 10-13 is respectfully requested.

In view of the foregoing, and in summary, claims 1-13 are considered to be in condition for allowance. Favorable reconsideration of this application, as amended, is respectfully requested.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this

paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

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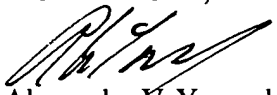

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